Code: R7221004 **R07**

B.Tech II Year II Semester (R07) Supplementary Examinations December/January 2015/2016

DIGITAL IC APPLICATIONS

(Electronics & Instrumentation Engineering)

(For 2008 Regular admitted batch only)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions
All questions carry equal marks

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1 (a) What are the advantages of CMOS logic family over bipolar logic family?
(b) Draw and explain the logic diagram for NAND and NOR gates using CMOS logic.

2 (a) Explain the operation of TTL NAND gate.
(b) Explain IC interfacing for CMOS and TTL interfacing.

3 (a) Explain the difference between a syntax error and schematic error.
(b) List the advantages of the VHDL methodology over traditional digital design.
(c) What is a signal source and what are the different kinds of signal sources?

4 (a) List the VHDL operators in detail.
(b) Can every VHDL program that can be simulated be synthesized? If not, explain.
(c) What are the basic inputs and outputs for an synthesizer?

5 (a) Write a VHDL description for full adder circuit by using structural model.
(b) Write VHDL description for BCD to EXCESS-3 CODE converter.

6 (a) Design and describe VHDL code for 3 to 8 decoder by using data flow model.
(b) Write a behavioral description of a 4 to 2 priority encoder.

7 (a) Write a behavioral description of a negative level edge triggered clocked SR latch.
(b) Write a VHDL description for 8 bit shift register.

8 (a) Draw and explain the internal architecture for DRAM.
(b) Draw and explain the timing diagram for synchronous static RAMS.

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